

**Amendments to the Claims:**

Following is a complete listing of the claims pending in the application, as amended:

1. (currently amended) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:
  - a semiconductor substrate;
  - a gate oxide formed on said semiconductor substrate;
  - a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;
  - an isolation layer formed over the sidewall of said gate structure and said substrate;
  - first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;
  - source and drain regions formed adjacent to said gate structure and under said undercut structure; and
  - salicide formed on said gate structure and said source and drain regions.
  
2. (original) The nonvolatile memory of Claim 1, further comprising pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.
  
3. (original) The nonvolatile memory of Claim 1, further comprising:
  - lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and
  - pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

4. (cancelled)

5. (original) The nonvolatile memory of Claim 1, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

6. (cancelled)

7. (cancelled)

8. (cancelled)

9. (original) The nonvolatile memory of Claim 1, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (original) The nonvolatile memory of Claim 1, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

14. (original) The nonvolatile memory of Claim 1, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

15. (original) The nonvolatile memory of Claim 1, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

16. (original) The nonvolatile memory of Claim 2, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

17. (original) The nonvolatile memory of Claim 2, wherein said wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

18. (original) The nonvolatile memory of Claim 2, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

19. (original) The nonvolatile memory of Claim 3, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

20. (original) The nonvolatile memory of Claim 3, wherein said wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

21. (original) The nonvolatile memory of Claim 3, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

22. (cancelled)

23. (cancelled)

24. (cancelled)

25. (currently amended) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into

said gate structure, wherein said gate structure comprising a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;  
a second dielectric layer formed over the sidewall of said gate structure and substrate;  
first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and  
source and drain regions formed adjacent to said gate structure and under said undercut structure.

26. (original) The nonvolatile memory of Claim 25, further comprising pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

27. (original) The nonvolatile memory of Claim 25, further comprising:  
lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and  
pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

28. (cancelled)

29. (original) The nonvolatile memory of Claim 25, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

30. (cancelled)

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (cancelled)

35. (cancelled)

36. (cancelled)

37. (original) The nonvolatile memory of Claim 25, wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

38. (original) The nonvolatile memory of Claim 25, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

39. (original) The nonvolatile memory of Claim 25, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{WSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

40. (original) The nonvolatile memory of Claim 25, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

41. (original) The nonvolatile memory of Claim 26, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

42. (original) The nonvolatile memory of Claim 26, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

43. (original) The nonvolatile memory of Claim 26, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{WSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

44. (original) The nonvolatile memory of Claim 26, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

45. (original) The nonvolatile memory of Claim 27, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

46. (original) The nonvolatile memory of Claim 27, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

47. (original) The nonvolatile memory of Claim 27, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{WSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

48. (original) The nonvolatile memory of Claim 27, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

49. (cancelled)

50. (cancelled)

51. (cancelled)

52. (cancelled)

53. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

54. (new) The nonvolatile memory of Claim 53, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

55. (new) The nonvolatile memory of Claim 53, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

56. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

57. (new) The nonvolatile memory of Claim 56, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

58. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and



lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

59. (new) The nonvolatile memory of Claim 58, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

60. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion

implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

61. (new) The nonvolatile memory of Claim 60, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

62. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

- a semiconductor substrate;
- a gate oxide formed on said semiconductor substrate;
- a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;
- a second dielectric layer formed over the sidewall of said gate structure;
- first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and
- source and drain regions formed adjacent to said gate structure and under said undercut structure;
- lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and
- pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than

6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

63. (new) The nonvolatile memory of Claim 62, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

64. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure;

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

65. (new) The nonvolatile memory of Claim 64, further comprising second spacers attached on said first spacers, wherein said second spacers is formed of oxide or the material having energy gap larger than 7eV.

66. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

- a semiconductor substrate;
- a gate oxide formed on said semiconductor substrate;
- a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;
- an isolation layer formed over the sidewall of said gate structure;
- first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;
- source and drain regions formed adjacent to said gate structure and under said undercut structure; and
- wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

67. (new) The nonvolatile memory of Claim 66, further comprising double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions.

68. (new) The nonvolatile memory of Claim 67, further comprising pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

69. (new) The nonvolatile memory of Claim 66, further comprising lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions.

70. (new) The nonvolatile memory of Claim 66, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

71. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

- a semiconductor substrate;

- a gate oxide formed on said semiconductor substrate;

- a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;

- a second dielectric layer formed over the sidewall of said gate structure;

- first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

- source and drain regions formed adjacent to said gate structure and under said undercut structure; and

- wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate is formed of oxide or the material having energy gap larger than 7eV.

72. (new) The nonvolatile memory of Claim 71, further comprising double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain

regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions.

73. (new) The nonvolatile memory of Claim 72, further comprising pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

74. (new) The nonvolatile memory of Claim 71, further comprising lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions.

75. (new) The nonvolatile memory of Claim 71, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

76. (new) A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

- a semiconductor substrate;
- a gate oxide formed on said semiconductor substrate;
- a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;
- an isolation layer formed over the sidewall of said gate structure;
- first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;
- source and drain regions formed adjacent to said gate structure and under said undercut structure;
- salicide formed on said gate structure and said source and drain regions;

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions; wherein said isolation layer is formed of oxide or the material having energy gap larger than 7 eV.

77. (new) The nonvolatile memory of Claim 76, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

78. (new) The nonvolatile memory of Claim 76, wherein said silicide material includes  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}$ .

79. (new) A nonvolatile memory with spacer trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure comprises a stacked structure including of polysilicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed on the sidewall of said gate structure and the surface of said semiconductor substrate;

first spacers formed on the sidewall of said second dielectric layer;

source and drain regions formed adjacent to said gate structure, wherein p-n junctions of said source and drain regions formed under said first spacers;

double doped drain region adjacent to said source and drain regions, wherein the p-n junctions of said double doped drain region are formed under said first spacers and the junction of said double doped drain region being deeper than the one of

said source and drain regions, said double doped drain region being closer to the channel under said gate structure than said source and drain regions and the doping concentration of said double doped drain region is lower than the one of said source and drain regions;

pocket ion implantation region adjacent to said double doped drain region, the conductive type of the pocket ion implantation region being opposite to the one of the source and drain regions; and

wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

80. (new) The nonvolatile memory of Claim 79, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

81. (new) The nonvolatile memory of Claim 79, wherein said silicide material includes TiSi<sub>2</sub>, WSi<sub>2</sub>, CoSi<sub>2</sub> or NiSi.

82. (new) The nonvolatile memory of Claim 79, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.